REMARKS

This paper is responsive to the Office Action mailed from the Patent and Trademark Office on May 24, 2005, which has a shortened statutory period set to expire August 24, 2005. A petition is filed herewith extending the period of response until November 24, 2005.

Claims 1-21 are pending in the above-identified application. Claims 1-21 are rejected under 35 USC 102 and/or 35 USC 103.

In the current paper, Claims 1, 16, and 21 are amended to clarify the claimed invention, Claims 2, 3, 5, 7 and 17-20 are canceled, and Claims 4, 6 and 8 are amended to depend from amended Claim 1. No new matter is entered. In view of these amendments and the following remarks, Applicants respectfully request reconsideration and withdrawal of all pending rejections.

Rejections Under 35 USC 102

Claims 1-3, 7, 16-18 and 20 are rejected under 35 USC 102(b) as being anticipated by European Patent #1079445 (herein "Sudou").

Claim 1 is amended to include the limitations of Claims 2, 3, 5 and 7, and as such now recites (in pertinent part):

> A microelectromechanical device comprising at least one thermoelectric layer on a substrate...
>
> wherein at least one stress reduction means is arranged between regions of at least one of a functional structure and a region with a thermoelectric layer, and
>
> wherein the stress reduction means comprises at least one of:
>
> (a) an antiadhesion layer for reducing or preventing the adhesion of material of the layer and thus for forming at least one stress reduction means,
>
> (b) a vertical offset between two laterally adjoining layers is arranged as said stress reduction means in at least one region on the substrate, and
>
> (c) at least one trench is arranged as said stress reduction means in at least one region of the substrate.

Sudou et al. (EP 1 079 445 A2) disclose a thermoelectric conversion device for converting heat into electricity and a method for manufacturing the device. The thermoelectric conversion device includes n-type and p-type thermoelectric elements 6, which are disposed between an upper and lower substrate 1,2 and are connected by electrodes 3,4. For the manufacturing of the thermoelectric conversion device (as described in Sudou's paragraphs 0029 to 0036, the elements are grown on the electrode wiring on the substrate using an electroplating method and a plating mask having holes, and an electrode junction layer is shaped on the elements. For the thermoelectric conversion device, n-type elements are grown on a first substrate and p-type elements on a second substrate, and the two substrates are joined together, such that the elements extend between the two substrates, and n-type and p-type elements alternate. The connection between the elements on the one substrate and the electrodes on the other substrate are established by the electrode junction layer, thus forming the thermoelectric conversion device.

The method disclosed by Sudou includes manufacturing a thermoelectric conversion device featuring a large number of thermoelectric electric elements connected in series. For this purpose, the thermoelectric conversion device is made of elements which are grown spatially separated by using a mask having holes. The method according to Sudou does not involve the creation of a continuous layer of a thermoelectric material, such that the problem of stress within the grown elements does not arise. Consequently the thermoelectric conversion device according to Sudou does not require stress reduction means. As such, Sudou fails to anticipate the structure of Claim 1 at least because Sudou fails to teach or suggest "wherein the stress reduction means comprises at least one of: (a) an antiadhesion layer for reducing or preventing the adhesion of material of the layer and thus for forming at least one stress reduction means, (b) a

vertical offset between two laterally adjoining layers is arranged as said stress reduction means in at least one region on the substrate, and (c) at least one trench is arranged as said stress reduction means in at least one region of the substrate", as recited in Claim 1.

The limitations of Claims 2, 3 and 7 are incorporated into Claim 1, and therefore Claims 2, 3 and 7 are canceled herein.

Although not formally rejected over Sudou on page 2 of the Office Action, the Examiner indicates that Claims 8-15 are also subject to rejection on pages 3 and 4 of the Office Action. Claims 8-15 are dependent from Claim 1, and are therefore distinguished over Sudou for at least the reasons provided above with reference to Claim 1.

Similar to Claim 1, Claim 16 is amended to include the limitations of Claims 17-20, whereby Claim 16 now recites (in pertinent part):

> A method for producing a thermoelectric semiconductor component, the method comprising...
>
> wherein forming the layer comprises forming a thermoelectric layer, and wherein the method further comprises arranging said at least one stress reduction means between regions of at least one of a functional structure and a region with a thermoelectric layer, and
>
> wherein forming the stress reduction means comprises at least one of:
>
> (a) forming an antiadhesion layer for reducing or preventing the adhesion of material of the layer and thus for forming at least one stress reduction means in at least one region of the substrate,
>
> (b) arranging a vertical offset between two laterally adjoining layers as said stress reduction means in at least one region on the substrate, and
>
> (c) producing at least one trench using at least one of mechanical and

chemical processes as said stress reduction means in at least one region of the substrate.

As amended, Claim 16 is believed to be distinguished over Sudou for reasons similar to those provided above with reference to Claim 1.

The limitations of Claims 17, 18 and 20 are incorporated into Claim 16, and therefore Claims 17, 18 and 20 are canceled herein.

For the above reasons, Applicants' respectfully request reconsideration and withdrawal of the rejections under 35 USC 102.

Rejections Under 35 USC 103

Claim 4 is rejected under 35 USC 103 as being unpatentable over Sudou in view of US Patent Published Application 20010009800 (Hijzen).

Hijzen is directed to the manufacture of trench-gate semiconductor devices, but does not mention the use of thermoelectric materials or materials with greatly differing thermal expansion coefficients. Accordingly, Hijzen fails to overcome the deficiencies associated with Sudou as directed to Claim 1 at least because Hijzen fails to teach or suggest the "stress reduction means" recited in Claim 1. Therefore, Claim 4, which is amended herein to depend from Claim 1, is distinguished over Sudou and Hijzen for the reasons set forth above.

Claims 5, 6 and 19 are rejected under 35 USC 103 as being unpatentable over Sudou in view of US Patent Published Application 2002015281 (Goldbach).

The limitations of Claim 5 is incorporated into Claim 1, and therefore Claim 5 is canceled herein. Similarly, the limitations of Claim 19 is incorporated into Claim 16, and therefore Claim 19 is canceled herein.

Goldbach is directed to a stress-reduced layer system, for example, in the manufacture of trench capacitors in DRAM memory cells. The stress reduction scheme taught by Goldbach is achieved, as described in Goldbach's paragraph 0031, by the controlled induction of impurities into a semiconductor layer, thus reducing the stresses at the interfaces of the layers. The properties of the impurities are chosen in such a way that the mechanical stresses are reduced, but the electrical properties of the layers are not altered.

As such, Goldbach fails to teach or suggest "wherein the stress reduction means comprises at least one of: (a) an antiadhesion layer for reducing or preventing the adhesion of material of the layer and thus for forming at least one stress reduction means, (b) a vertical offset between two laterally adjoining layers is arranged as said stress reduction means in at least one region on the substrate, and (c) at least one trench is arranged as said stress reduction means in at least one region of the substrate", as recited in Claim 1. Therefore, Claim 6, which is amended herein to depend from Claim 1, is distinguished over Sudou and Hijzen for the reasons set forth above.

Similarly, Goldbach fails to teach or suggest "wherein forming the stress reduction means comprises at least one of: (a) forming an antiadhesion layer for reducing or preventing the adhesion of material of the layer and thus for forming at least one stress reduction means in at least one region of the substrate, (b) arranging a vertical offset between two laterally adjoining layers as said stress reduction means in at least one region on the substrate, and (c) producing at least one trench using at least one of mechanical and chemical processes as said stress reduction means in at least one region of the substrate", as recited in Claim 16.

Claim 21 is rejected under 35 USC 103 as being unpatentable over Sudou in view of US Patent 5,547,598 (Amano).

Similar to Claims 1 and 16, Claim 21 is amended to recite (in pertinent part):

> 21. (currently amended) A microelectromechanical device ...
> wherein each stress reduction region comprises at least one of:
> (a) an antiadhesion layer for reducing or preventing the adhesion of material of the layer and thus for forming at least one stress reduction means,
> (b) a vertical offset between two laterally adjoining layers is arranged as said stress reduction means in at least one region on the substrate, and
> (c) at least one trench is arranged as said stress reduction means in at least one region of the substrate.

Support for the amendment to Claim 21 is provided in Claims 2, 3, 5 and 7 (as filed). No new matter is entered.

As amended, Claim 21 is believed to be distinguished over Sudou for reasons similar to those provided above with reference to Claim 1.

Amano dislcoses a thermoelectric semiconductor material comprising an Si crystal and a crystal of metal siliicide, preferably β-$FeSi_2$. Amano teaches the addition of other elements as additives and serving as dopants. In this way it is possible to create a thermoelectric material, which has a large Seebeck-coefficient and at the same time a relatively small electrical resistance, thus allowing for a large output power of respective thermoelectric elements. However, Amano is distinguished over the method of Claim 21 at least because Amano fails to teach or suggest "wherein said at least one thermoelectric layer is divided into a plurality of thermoelectric layer portions, each thermoelectric layer portion being separated from adjacent thermoelectric layer portions by a stress reduction region, and ... wherein each stress reduction region comprises at least one of: (a) an antiadhesion layer for reducing or preventing the adhesion of material of the layer and thus for forming at least one stress reduction means, (b) a vertical offset between two

laterally adjoining layers is arranged as said stress reduction means in at least one region on the substrate, and (c) at least one trench is arranged as said stress reduction means in at least one region of the substrate", as recited in Claim 21. Accordingly, it would have been neither possible nor obvious to combine the teachings of Sudou and Amano to produce the method of Claim 21.

For the above reasons, Applicants' respectfully request reconsideration and withdrawal of the rejections under 35 USC 103.

CONCLUSION

For the above reasons, Applicants believe Claims 1, 4, 6, 8-16 and 21 are believed to be in condition for allowance. Should the Examiner have any questions regarding the present paper, the Examiner is invited to contact the undersigned attorney at the number provided below.

Respectfully submitted,

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I hereby certify that this correspondence is being deposited with the United States Postal Service as FIRST CLASS MAIL in an envelope addressed to: Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on November 21, 2005.

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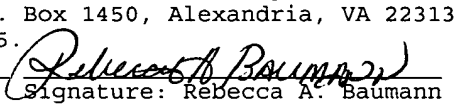
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